

ABSTRACT

The present invention discloses an optimal hardware implementation of the FFT/IFFT operation that minimizes the number of clock cycles required to compute the FFT/IFFT while at the same time minimizing the number of complex multipliers needed. For performing an N-point FFT/IFFT operation in N clock cycles, the optimal hardware implementation consists of several modules. An input module receives a plurality of inputs in parallel and combines the inputs after applying a multiplication factor to each of the inputs. At least one multiplicand generator is used to provide multiplicands to the system. At least two complex multiplier modules for performing complex multiplications are required with at least one of the complex multiplier modules receiving an output from the input module. Each of the complex multiplier modules receives multiplicands from the at least one multiplicand generator. Furthermore, at least one of the complex multiplier modules receives an output of another complex multiplier module. A map module is provided for receiving outputs of the at least two complex multiplier modules, the map module selecting and applying a multiplication factor to each of the outputs received to generate multiple outputs. Finally, an accumulation module receives and performs an accumulation task on each of the multiple outputs of the map module thereby generating a corresponding number of multiple outputs. In a preferred embodiment, the N-point FFT/IFFT operation is performed in N clock cycles using $\left(\frac{N}{32} + 1\right)$ complex multipliers. In a specific implementation, a system comprising 3 complex multipliers is used to compute a 64-point FFT/IFFT operation in 64 clock cycles. Advantageously, the total number of clock cycles required to complete the FFT/IFFT operation is minimized while at the same time minimizing the number of complex multipliers needed.